PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Farnworth et al.

Serial No.: 10/690,417

Filed: October 20, 2003

For: METHODS OF COATING AND SINGULATING WAFERS (as amended)

Confirmation No.: 3773

Examiner: P. Perkins

Group Art Unit: 2822

Attorney Docket No.: 2269-5947US
(03-0316.00/US)

Notice of Allowance Mailed:

December 1, 2005

NOTICE OF EXPRESS MAILING

Express Mail Mailing Label Number: EL995988961US

Date of Deposit with USPS: March 1, 2006

Person making Deposit: Timothy Palfreyman

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In the Office Action dated August 4, 2005, the Examiner indicates:

The following is a statement of reasons for the indication of allowable subject matter: referring to claim 18, prior art does not disclose, teach or suggest etching the passive surface of the semiconductor wafer such that the first protective coating exposed within the at least one channel forms at least one frame element protruding from the passive surface of the semiconductor wafer; and anchoring the second protective coating to the passive surface of the semiconductor wafer with the at least one frame element.

Referring to claim 38, prior art does not disclose, teach or suggest etching the passive surface of the semiconductor wafer concurrently with etching the plurality of semiconductor die side surfaces.

In the Notice of Allowance dated December 1, 2005, the Examiner indicates:

Prior art does not anticipate, teach, or suggest referring to claim 1, prior art does not disclose, teach or suggest etching the passive surface of the semiconductor wafer such that the first protective coating exposed within the at least one channel forms at least one frame element protruding from the passive surface of the semiconductor wafer; and anchoring the second protective coating to the passive surface of the semiconductor wafer with the at least one frame element.

Referring to Claim 21, prior art does not disclose, teach or suggest etching the plurality of semiconductor die side surfaces to remove a layer of semiconductor material containing cutting-induced defects and to expose the first protective coating within the at least one channel; forming a second protective coating on the semiconductor wafer to cover the passive surface and fill the at least one channel; and separating the semiconductor wafer along the at least one channel to form a plurality of individual chip-scale packages.

Referring to claim 38, prior art does not disclose, teach or suggest etching the passive surface of the semiconductor wafer concurrently with etching the plurality of semiconductor die side surfaces.

For example, Takahashi et al. (5,977,641) disclose a method of forming chip-scale packages including providing a semiconductor wafer having an active surface with a plurality of semiconductor die locations separated by at least one street of semiconductor material; cutting at least one channel in the active surface of the semiconductor wafer along the at least one street of semiconductor material to expose a plurality of semiconductor die surfaces; forming a protective coating on the semiconductor wafer to cover the active surface and fill the at least one channel; and separating the semiconductor wafer along the at least one channel to form a plurality of individual chip-scale packages.

However, Takahashi et al. do not disclose, anticipate, teach or suggest etching the plurality of semiconductor die side surfaces to remove a layer of semiconductor material containing cutting-induced defects and to expose the first protective coating within the at least one channel; etching the passive surface of the semiconductor wafer such that the first protective coating exposed within the at least one channel forms at least one frame element protruding from the passive surface of the semiconductor wafer, wherein etching the passive surface of the semiconductor wafer is done concurrently with etching the plurality of semiconductor die side surfaces; forming a second protective coating on the

semiconductor wafer to cover the passive surface and fill the at least one channel and anchoring the second protective coating to the passive surface of the semiconductor wafer with the at least one frame element.

Shelton et al. (6,849,524) disclose a method of forming chip-scale packages including providing a semiconductor wafer having an active surface with a plurality of semiconductor die locations separated by at least one street of semiconductor material; forming a protective coating on the semiconductor to cover the active surface (Step 410); cutting at least one channel in the active surface of the semiconductor wafer along the at least one street of semiconductor material to expose a plurality of semiconductor die surfaces (Step 440); etching the plurality of semiconductor die side surfaces to remove a layer of semiconductor material containing cutting-induced defects (Step 550); and separating the semiconductor wafer along the at least one channel to form a plurality of individual chip-scale packages (Step 560).

However, Shelton et al., do not disclose, anticipate, teach or suggest etching the passive surface of the semiconductor wafer such that the first protective coating exposed within the at least one channel forms at least one frame element protruding from the passive surface of the semiconductor wafer, wherein etching the passive surface of the semiconductor wafer is done concurrently with etching the plurality of semiconductor die side surfaces; forming a second protective coating on the semiconductor wafer to cover the passive surface and fill the at least one channel and anchoring the second protective coating to the passive surface of the semiconductor wafer with the at least one frame element.

The prior art made of record in this action does not anticipate, teach, or suggest etching the plurality of semiconductor die side surfaces to remove a layer of semiconductor material containing cutting-induced defects and to expose the first protective coating within the at least one channel; etching the passive surface of the semiconductor wafer such that the first protective coating exposed within the at least one channel forms at least one frame element protruding from the passive surface of the semiconductor wafer, wherein etching the passive surface of the semiconductor wafer is done concurrently with etching the plurality of semiconductor die side surfaces; forming a second protective coating on the semiconductor wafer to cover the passive surface and fill the at least one channel and anchoring the second protective coating to the passive surface of the semiconductor wafer with the at least one frame element.

Applicants concur with the reasons as stated by the Examiner insofar as they comprise a summary, and are exemplary and not limiting. However, the independent claims as allowed include other and different language than that specified by the Examiner, and the allowed dependent claims include other and further features and elements. Accordingly, the scope of the claims must be determined from the literal language of each as a whole, as well as equivalents thereof.

Additionally, claim 18 was canceled and incorporated into claim 1. Claim 38 was canceled and rewritten in independent form as claim 46. Applicants agree with the characterization of the cited references as stated by the Examiner insofar as they comprise a summary, and are exemplary and not limiting. Applicants further refer to the arguments presented during prosecution of the above-entitled application.

Respectfully submitted,

Krista Weber Powell
Registration No. 47,867
Attorney for Applicants
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: March 1, 2006
KWP/dn:lmh
Document in ProLaw

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Farnworth et al.

Serial No.: 10/690,417

Filed: October 20, 2003

For: METHODS OF COATING AND SINGULATING WAFERS (as amended)

Confirmation No.: 3773

Examiner: P. Perkins

Group Art Unit: 2822

Attorney Docket No.: 2269-5947US

Notice of Allowance Mailed:

December 1, 2005

NOTICE OF EXPRESS MAILING

Express Mail Mailing Label Number: EL995988961US

Date of Deposit with USPS: March 1, 2006

Person making Deposit: Timothy Palfreyman

TRANSMITTAL LETTER

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants submit herewith Part B - Fee(s) Transmittal for the above-captioned application and a check in the amount of $1,715.00 in payment therefor plus five (5) copies of the patent when issued.

Also, enclosed is an Amendment Pursuant to 37 C.F.R. § 1.312(a) (14 pages); Comments on Statement of Reasons for Allowance (4 pages); and Fee Addressee for Receipt of PTO Notices Relating to Maintenance Fees (2 pages).

Applicants understand that no additional fees are required. However, if the Office determines that any comparison fees or other additional fees are required, the Commissioner is authorized to charge any such fees to TraskBritt Deposit Account No. 20-1469. A copy of this Transmittal Letter is enclosed for deposit account charging purposes.

Respectfully submitted,

Krista Weber Powell
Registration No. 47,867
Attorney for Applicants
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: March 1, 2006
KWP/dn:lmh
Enclosures: Part B - Issue Fee Transmittal (1 page)
Check No. 22581 in the amount of $1,715.00
Copy of Transmittal Letter (2 pages)
Amendment Pursuant to 37 C.F.R. § 1.312(a) (14 pages)
Comments on Statement of Reasons for Allowance (4 pages)
Fee Addressee for Receipt of PTO Notices Relating to Maintenance Fees (2 pages)
Document in ProLaw